Abstract

In an illustrative embodiment, a desired signal processing transfer function is implemented using a generic pipelined data processor having variable latency followed by a variable latency multistage FIFO. The delay of the multistage FIFO is varied dynamically to keep the number of outstanding samples (and thus the overall latency) a constant. The present invention enables an abstract approach to the design of higher-level signal processing transfer functions while the design of the underlying low-level circuitry is driven solely by target implementation technology issues. Thus, the higher-level design of signal processing transfer functions is decoupled from the low-level (logic and physical) design. Furthermore, test bench modules and vectors for testing the transfer function can also be to be prepared independent of the specifics of the low-level circuitry associated with the target implementation technology. The transfer functions of the present invention may be readily mapped onto any of multiple target implementation technologies. The inventive approach also permits changes in an underlying arithmetic library to be made without requiring changes in the higher-level signal processing transfer function design.